

# BUK7610-55AL

N-channel TrenchMOS standard level FET

Rev. 02 — 9 January 2008

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using NXP General-Purpose Automotive (GPA) TrenchMOS technology specifically optimized for linear operation. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features

- 175 °C rated
- Stable operation in linear mode
- Q101 compliant
- TrenchMOS technology

### 1.3 Applications

- 12 V and 24 V loads
- DC linear motor control
- Automotive systems
- Repetitive clamped inductive switching

### 1.4 Quick reference data

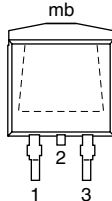
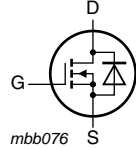
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 4</a> and <a href="#">1</a>	[1]	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	300	W
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped inductive load	-	-	1.1	J
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	8.5	10	m $\Omega$

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT404 (D2PAK)**

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK7610-55AL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

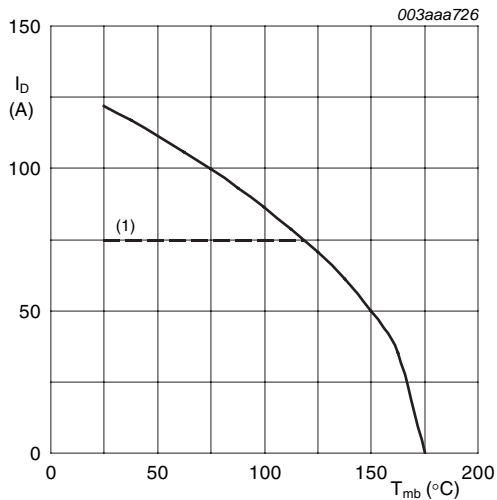
## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	55	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 4</a> and <a href="#">1</a>	<a href="#">[1][2]</a>	122	A
		$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 4</a> and <a href="#">1</a>	<a href="#">[3]</a>	75	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 4</a>	<a href="#">[3]</a>	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed	-	490	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	300	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped inductive load	-	1.1	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see <a href="#">Figure 3</a>	<a href="#">[4][5]</a> <a href="#">[6]</a>	-	J
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	<a href="#">[1][2]</a>	122	A
		$T_{mb} = 25\text{ °C}$	<a href="#">[3]</a>	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	490	A

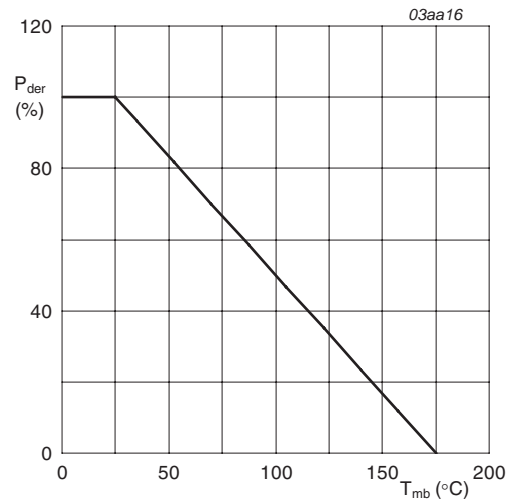
- [1] Current is limited by power dissipation chip rating.
- [2] Refer to document 9397 750 12572 for further information.
- [3] Continuous current is limited by package.
- [4] Single shot avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Repetitive avalanche rating limited by average junction temperature of 170 °C.
- [6] Refer to application note AN10273 for further information.



$V_{GS} \geq 10 V$

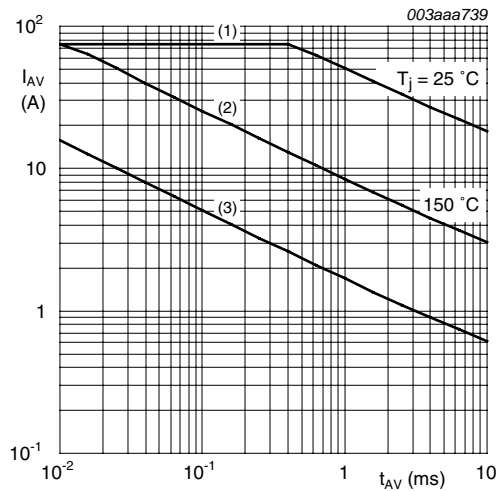
(1) Capped at 75 A due to package.

**Fig 1. Continuous drain current as a function of mounting base temperature**



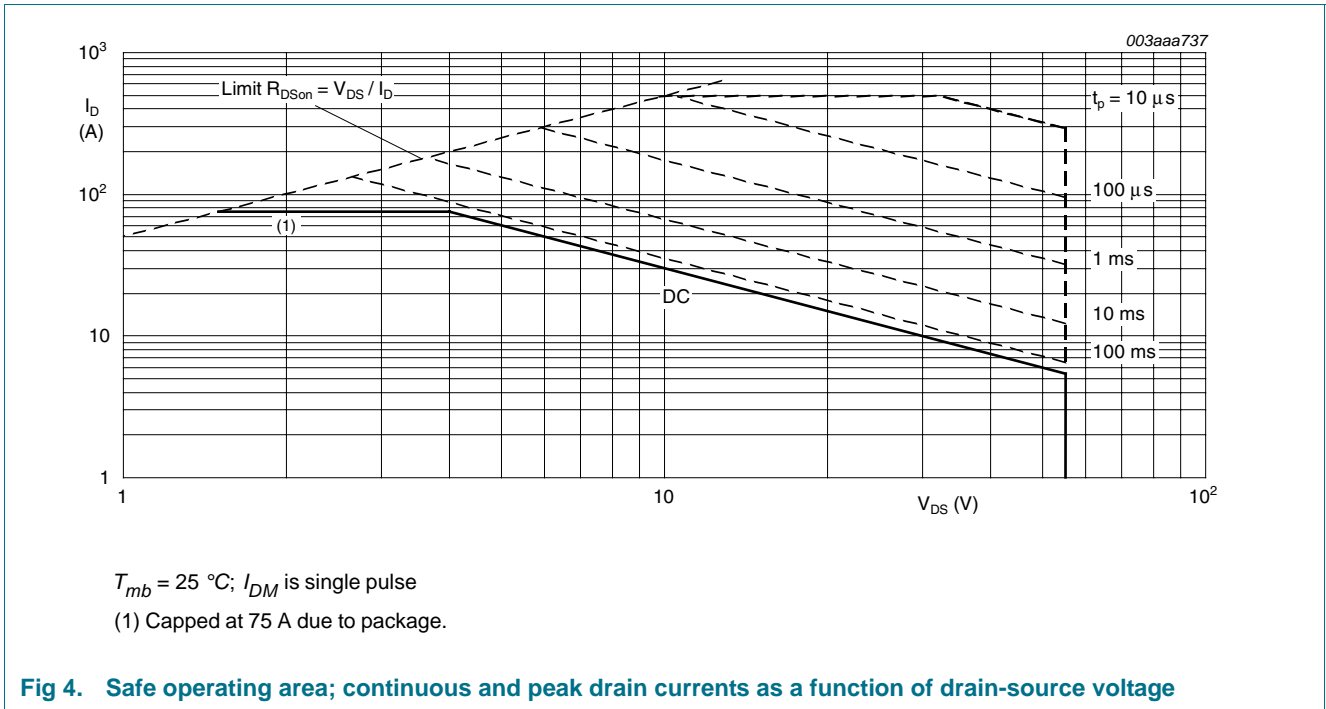
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100 \%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



- (1) Single-shot.
- (2) Single-shot.
- (3) Repetitive.

**Fig 3. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period**



## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	0.25	0.5	K/W

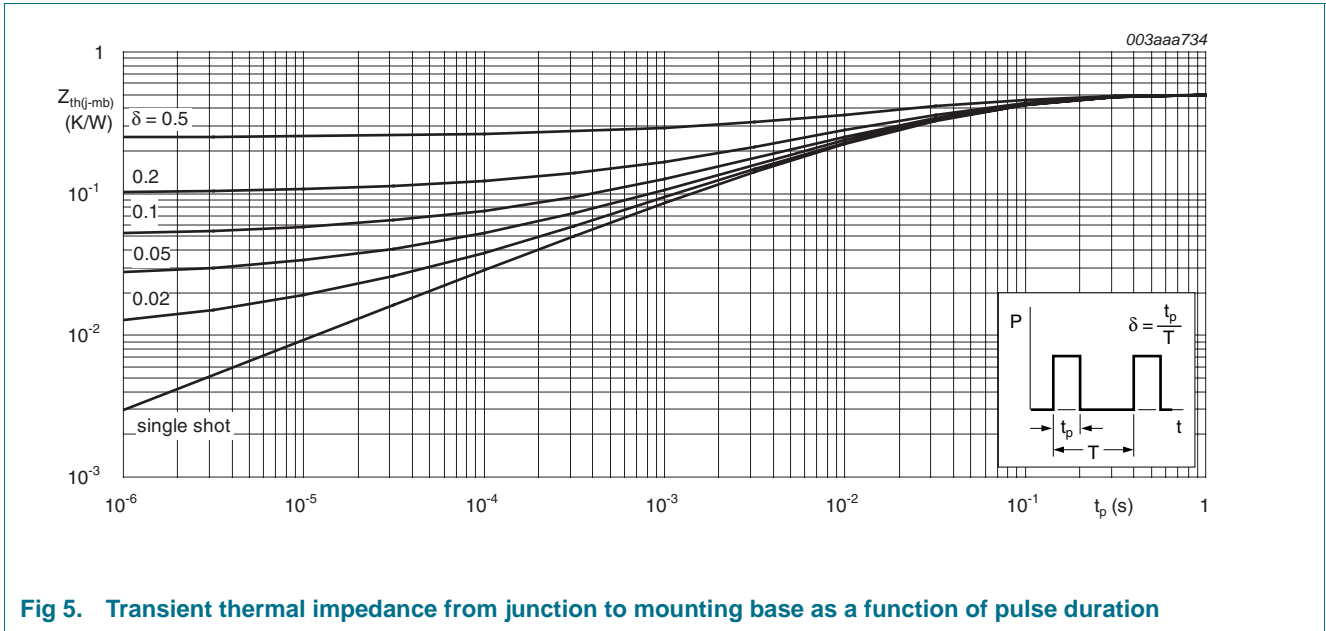


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

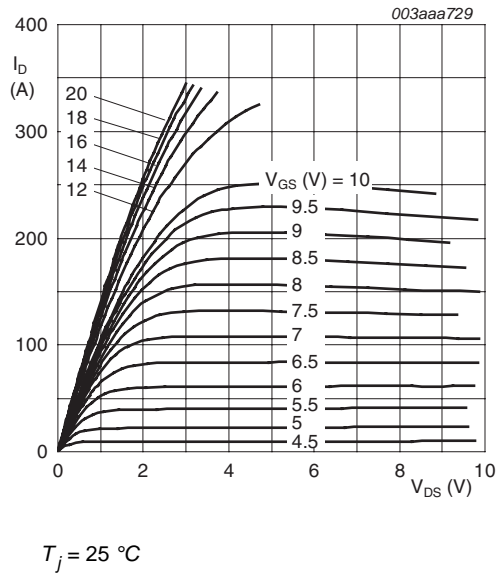
## 6. Characteristics

Table 6. Characteristics

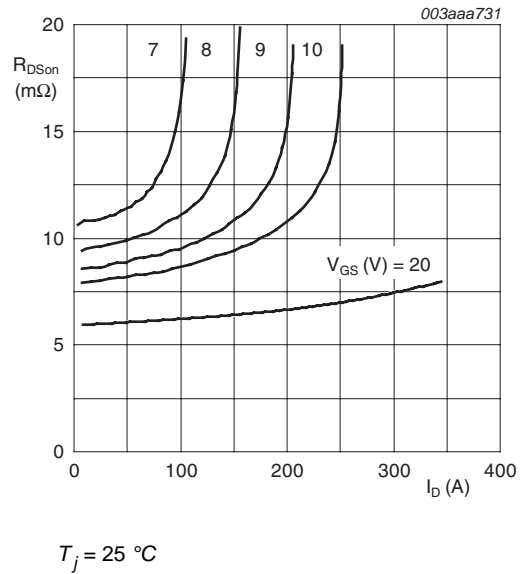
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	50	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> and <a href="#">11</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> and <a href="#">11</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> and <a href="#">11</a>	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.05	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = +20 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	-	20	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	8.5	10	m $\Omega$

Table 6. Characteristics ...continued

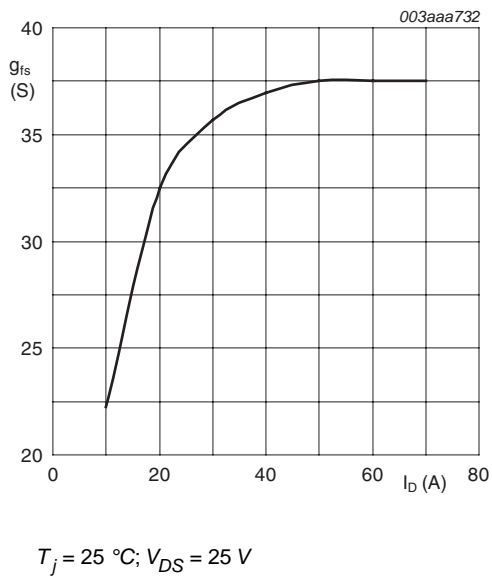
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 16</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ °C}$	-	73	-	ns
$Q_r$	recovered charge	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ °C}$	-	430	-	nC
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25\text{ A}$ ; $V_{DS} = 44\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 14</a>	-	124	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}$ ; $V_{DS} = 44\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 14</a>	-	22	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 44\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 14</a>	-	50	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 25\text{ A}$ ; $V_{DS} = 44\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 14</a>	-	5	-	V
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 15</a>	-	4710	6280	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 15</a>	-	980	1180	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 15</a>	-	560	770	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 30\text{ V}$ ; $R_L = 1.2\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $R_{G(\text{ext})} = 10\ \Omega$ ; $T_j = 25\text{ °C}$	-	33	-	ns
$t_r$	rise time	$V_{DS} = 30\text{ V}$ ; $R_L = 1.2\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $R_{G(\text{ext})} = 10\ \Omega$ ; $T_j = 25\text{ °C}$	-	117	-	ns
$t_{d(\text{off})}$	turn-off delay time	$V_{DS} = 30\text{ V}$ ; $R_L = 1.2\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $R_{G(\text{ext})} = 10\ \Omega$ ; $T_j = 25\text{ °C}$	-	132	-	ns
$t_f$	fall time	$V_{DS} = 30\text{ V}$ ; $R_L = 1.2\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $R_{G(\text{ext})} = 10\ \Omega$ ; $T_j = 25\text{ °C}$	-	95	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to center of die; $T_j = 25\text{ °C}$	-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad; $T_j = 25\text{ °C}$	-	7.5	-	nH



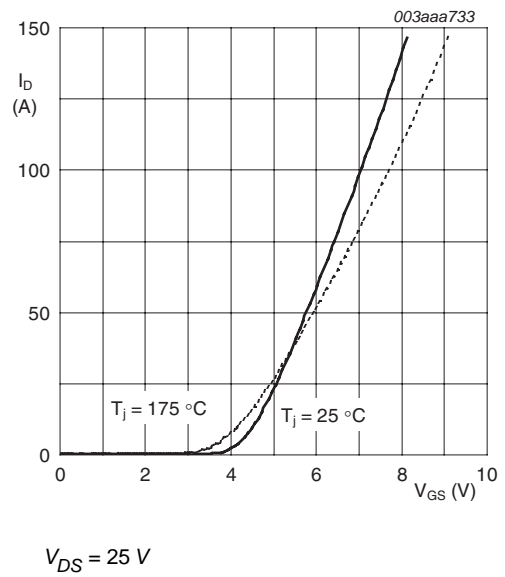
**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



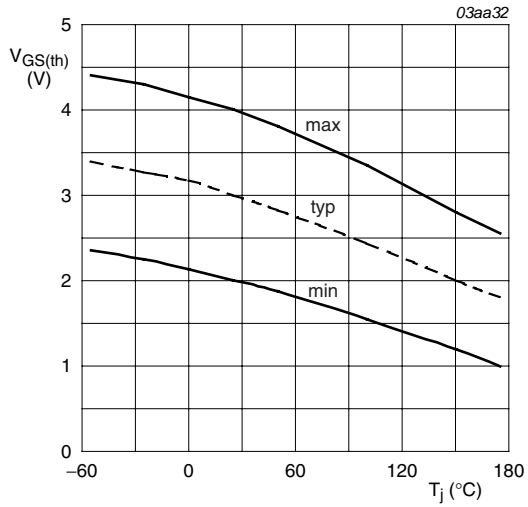
**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**



**Fig 8. Forward transconductance as a function of drain current; typical values**

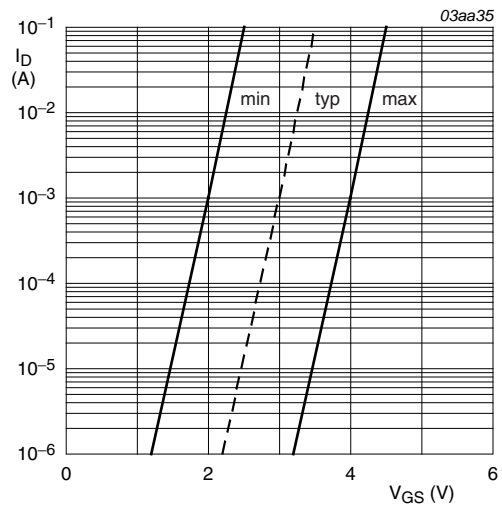


**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



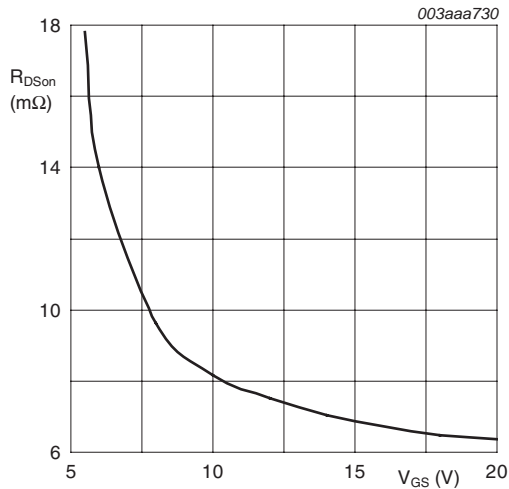
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**



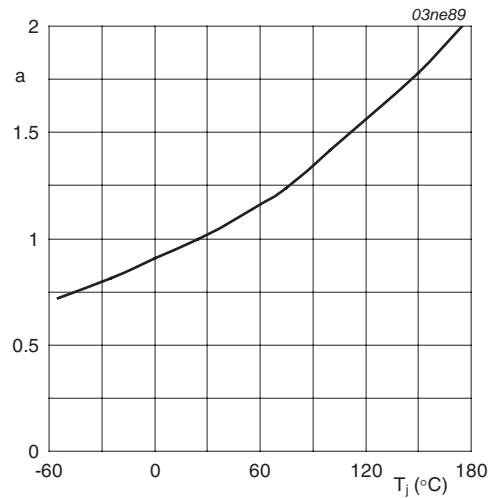
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

**Fig 11. Sub-threshold drain current as a function of gate-source voltage**



$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$

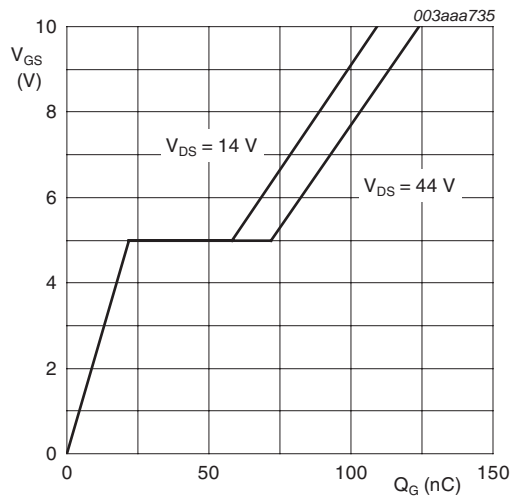
**Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$$a = \frac{R_{DSon}}{R_{DSon(25\text{°C})}}$$

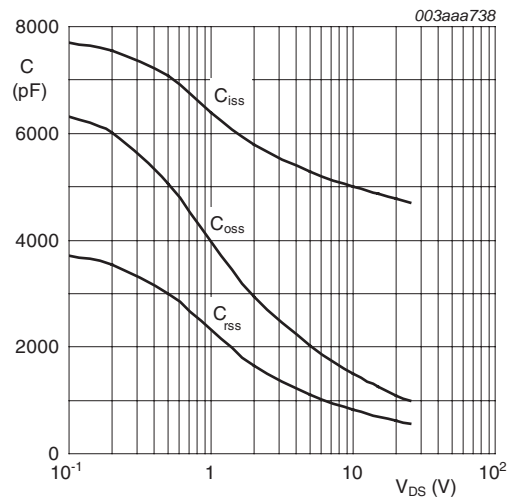
**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**





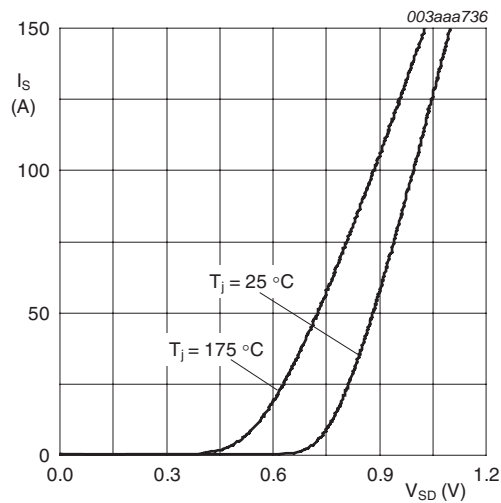
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



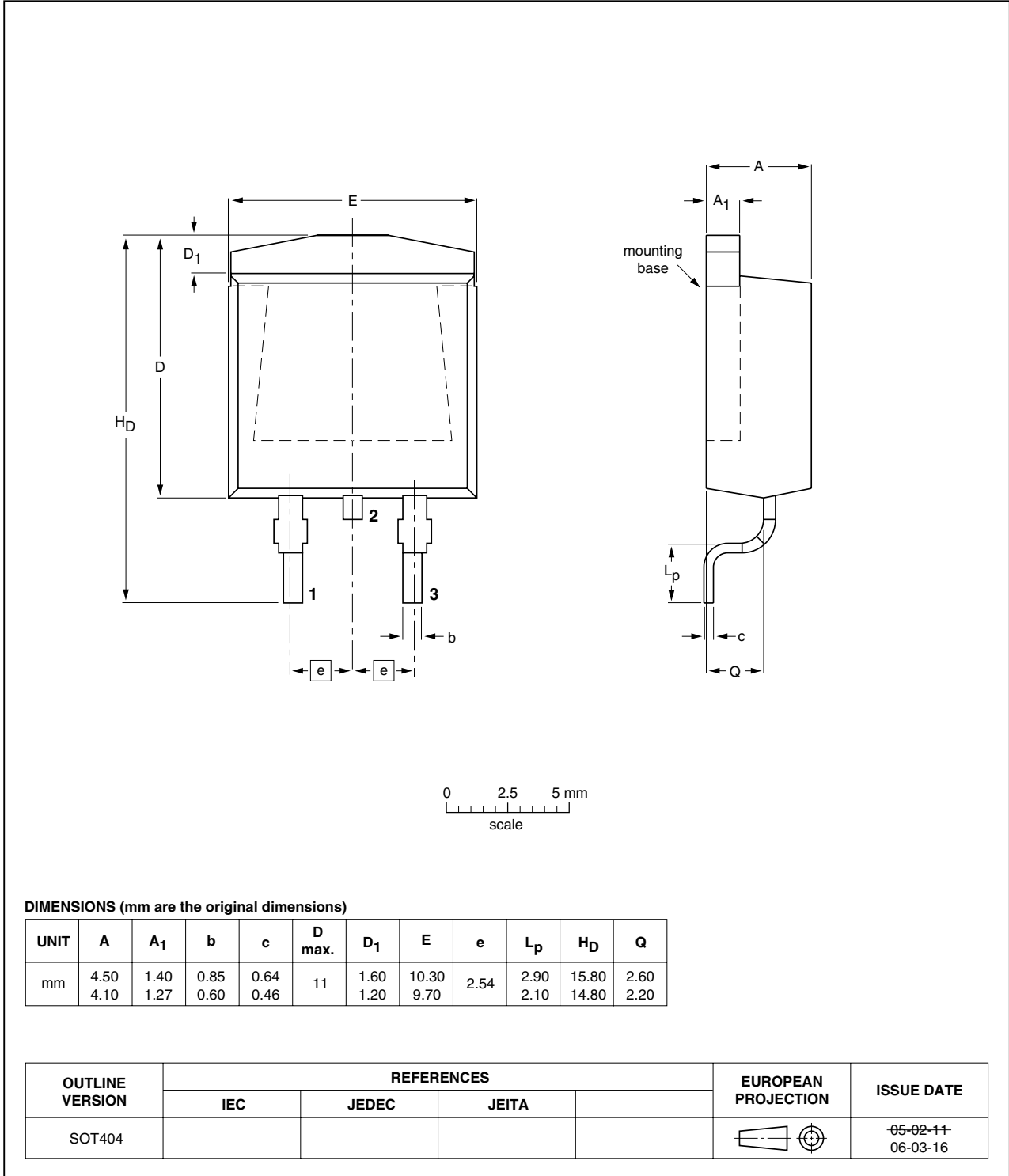
$V_{GS} = 0\text{ V}$

**Fig 16. Source current as a function of source-drain voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

**SOT404**



**Fig 17. Package outline SOT404 (D2PAK)**

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7610-55AL_2	20080109	Product data sheet	-	BUK75_7610_55AL_1
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Typical thermal resistance (j-mb) figure added in <a href="#">Table 5</a>.</li></ul>		
BUK75_7610_55AL_1	20041022	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 9 January 2008

Document identifier: BUK7610-55AL\_2